

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	10800829
Filing Date	2004-03-15
First Named Inventor	Newton G. Peterson
Art Unit	2643
Examiner Name	Unknown
Attorney Docket Number	5150-65801

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	1	TAREK ABDELZAHER, ELLA M. ATKINS and KANG G. SHIN; "QoS Negotiation in Real-Time Systems and Its Application to Automated Flight Control"; IEEE Transactions on Computers; November 2000; pages 1170-1183.	<input type="checkbox"/>
	2	HUGO A. ANDRADE and SCOTT KOVNER; "Software Synthesis from Dataflow Models for G and LabVIEW"; Thirty-Second Asilomar Conference on Signals, Systems & Computers; November 1998; pages 1705-1709.	<input type="checkbox"/>
	3	JOSEPH TOBIN BUCK; "Scheduling dynamic dataflow graphs with Bounded Memory Using the Token Flow Model"; PhD Thesis, University of California at Berkeley; 1993; http://ptolemy.eecs.berkeley.edu/papers/jbuckThesis ;	<input type="checkbox"/>
	4	GIORGIO BUTTAZZO and LUCA ABENI; "Adaptive Rate Control through Elastic Scheduling"; IEEE Conference on Decision and Control; December 2000; pages 4883 - 4888.	<input type="checkbox"/>
	5	BRENDON CAHOON and KATHRYN S. MCKINLEY; "Data Flow Analysis for Software Prefetching Linked Data Structures in Java"; International Conference on Parallel Architectures and Compilation Techniques; 2001; pages 280 - 291.	<input type="checkbox"/>
	6	PO-YUNG CHANG, Eric HAO and YALE N. PATT; "Target Prediction for Indirect Jumps" 24th Annual International Symposium on Computer Architecture; 1997; pages 274 - 283.	<input type="checkbox"/>
	7	MARIUS EVERS, SANJAY J. PATEL, ROBERT S. CHAPPELL and YALE N. PATT; "An Analysis of Correlation and Predictability: What Makes Two Level Branch Predictors Work"; 25th Annual International Symposium on Computer Architecture; 1998; pages 52 - 61.	<input type="checkbox"/>
	8	EDWARD A. LEE and THOMAS M. PARKS; "Dataflow Process Networks"; in Proceedings of the IEEE; March 27, 1995; pages 773 - 801.	<input type="checkbox"/>

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9	ZHONG WANG, TIMOTHY W. O'NEIL, and EDWIN HSING-MEAN SHA, "Optimal Loop Scheduling for Hiding Memory Latency Based on Two-Level Partitioning and Prefetching" IEEE Transactions on Signal Processing; November 2001; pages 2853 - 2864.	<input type="checkbox"/>
10	TSE-YU YEH and YALE N. PATT; "Alternative Implementations of Two-Level Adaptive Branch Prediction"; 19th Annual International Symposium on Computer Architecture; 1992; pages 124 - 134.	<input type="checkbox"/>
11	T.-Y. Yeh and Y. N. Patt; "Two-level adaptive training branch prediction"; Proceedings of the 24th Annual ACM/IEEE International Symposium on Microarchitecture; 1991; pages 51-61.	<input type="checkbox"/>
12	NEWTON G. PETERSEN and MARTIN R. WOJCIK; "Feasibility Analysis of Caller Prediction"; March 21, 2002; 4 pages; The Department of Electrical and Computer Engineering – The University of Texas at Austin.	<input type="checkbox"/>
13	NEWTON G. PETERSEN and MARTIN R. WOJCIK; "Node Prefetch Prediction in Dataflow Graphs – Literature Survey"; March 25, 2002; 9 pages; The Department of Electrical and Computer Engineering – The University of Texas at Austin.	<input type="checkbox"/>
14	NEWTON G. PETERSEN and MARTIN R. WOJCIK; "Node Prefetch Prediction in Dataflow Graphs – Final Presentation" April 29, 2002; 9 pages; The Department of Electrical and Computer Engineering – The University of Texas at Austin.	<input type="checkbox"/>
15	NEWTON G. PETERSEN and MARTIN R. WOJCIK; "Node Prefetch Prediction in Dataflow Graphs – Final Report"; May 8, 2002; The Department of Electrical and Computer Engineering – The University of Texas at Austin.	<input type="checkbox"/>
16	KURT KEUTZER; "Lecture 9: Digital Signal Processors: Applications and Architectures"; Computer Science 252, Spring 2000.	<input type="checkbox"/>
17	DAVID B. SKILLICORN and DOMENICO TALIA; "Models and Languages for Parallel Computation"; ACM Computing Surveys; October 1996; 55 pages; Vol. 30, No. 2.	<input type="checkbox"/>
18	ZHONG WANG, MICHAEL KIRKPATRICK and EDWING HSING-MEAN SHA; "Optimal Two Level Partitioning and Loop Scheduling for Hiding Memory Latency for DSP Applications"; Design Automation Conference; 2000; 5 pages.	<input type="checkbox"/>
19	PIET WAUTERS, MARC ENGELS, RUDY LAUWEREINS and J.A. PEPPERSTRAETE; "Cyclo-Dynamic Dataflow"; 4th EUROMICRO Workshop on Parallel and Distributed Processing; January, 1996; pages 319 - 326.	<input type="checkbox"/>

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20	STEPHEN EDWARDS, LUCIANO LAVAGNO, EDWARD A. LEE and ALBERTO SANGIOVANNI-VINCENTELLI; "Design of Embedded Systems: Formal Models, Validation, and Synthesis"; Proceedings of the IEEE; March 1997; pages 366-387; Vol. 85, Iss. 3.	<input type="checkbox"/>
21	NEWTON G. PETERSEN and MARTIN R. WOJCIK; "Node Prefetch Prediction in Dataflow Graphs"; IEEE Workshop on Signal Processing Systems; October 2004; pages 310-315.	<input type="checkbox"/>

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey C. Hood/	Date (YYYY-MM-DD)	2007-03-09
Name/Print	Jeffrey C. Hood	Registration Number	35,198

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